IN THE SPECIFICATION:

The paragraph beginning on page 6, line 21 has been amended as follows:

--That is, if the Enable0 signal (202) is asserted ~~deasserted~~ and the Enable1 signal (201) is deasserted ~~asserted~~, the CPUCore1 (102) can use the CPUBus1 (108) monopolistically. On the other hand, the Enable0 signal (202) is deasserted ~~asserted~~ and the Enable1 signal (201) is asserted ~~deasserted~~, the external CPU 103 can use the CPUBus1 (108) monopolistically. In addition, in this embodiment, CPUs, which have the same architecture, are adopted for the internal CPU core and the external CPU, so that common programs stored in ROM can be used for both internal and external CPUs. --